CERTIFIED IN ADVANCED DIPLOMA IN ASIC DESIGN & VERIFICATION

Contact: 9640648777

Duration: 120 days

ADVANCE DIGITAL ELECTRONICS

- Introduction to VLSI
- ASIC Design Flow
- Logic Gates
- Number Systems and Code Conversions
- K-maps
- Combinational Logic Circuits
- Sequential Logic Circuits
- Flip-Flops
- Counters
- Registers
- Finite State Machine
- Memory Organizations
- Programmable Logic Devices (FPGA's)

LINUX

- Introduction to Linux OS
- Basics of Linux commands
- Basics of Shell scripting
- Basics of Perl scripting

VERILOG HDL

- Introduction to Verilog HDL
- Modeling Concepts
- Gate Level Modeling
- Data Flow Modeling
- Behavioural Modeling
- Structural Modeling
- Switch Level Modeling
  - Data Types
  - Operators
  - Procedure and Flow Of Control Statement
- Designing of Combinational Circuits
- Designing of Sequential Circuits
- FSM Design Modeling
- Designing of Memories
- Writing Testbench using Verilog
- Task and Functions
- System Tasks
- Compiler Directives
- Advance Nets in Verilog
- Bus Functional Modeling
- Verilog Based Assertions
- Code Coverage & FPGA Implementation

SYSTEM VERILOG& UVM

- Introduction to Verification Plan
- Introduction to System Verilog
- Data types
- Procedural & Flow Control Statements
- Arrays
- Task And Functions
- Interfaces and Clocking Block
- Program Blocks
- Fork – Join Statements
- OOPS Concepts
- Randomization and Constraints
- Mailboxes
- Semaphores
- Events
- Virtual Interfaces
- Assertions
- Functional Coverage
- Packages
- Writing Testbench in System Verilog
- Project supported based on Methodology

EDA TOOLS

- QuestaSim
- Modelsim
- Xilinx ISE

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PHYSICAL DESIGN

Trends And Challenges In VLSI
ASIC Flow
Introduction of Transistors
Introduction of CMOS Technology
Stick Diagrams
Lambda – Rules
Layouts

STA (STATIC TIMING ANALYSIS)

Fundamentals of Delay calculations (wire modeling).
Setup/Hold Time definitions & Slack Calculations.
Different Timing Path Analysis.
Analysis & approach to minimize the timing violations.
STA Constraint development.

PLACE & ROUTE

Floor Planning
I/O Ring & Power Grid Planning
Placement Methodologies
CTS(Clock Tree Synthesis)
Routing & Timing Optimization

DFT (DESIGN FOR TESTABILITY)

Fault Models
ATPG Algorithms
At-Speed Testing
IDDQ Testing & Memory BIST
I/O Testing
Pattern Generation

ARCHITECTURE

SOC Bus Structure
SOC Processor Architecture
SOC peripherals

LOGIC DESIGN

FSM Design & FIFO Design
Handshaking Protocol's
Math Function Implementation
Reset Design
Clock Management

EDA TOOLS

Micro Wind – Layout
DSCH – Schematics
H-Spice & Spice Language(optional)